## REMARKS

### I. CLAIM STATUS

Claims 1-8, 10-12, and 14-19 were pending. Claims 12, 14 and 17 have been canceled. Claims 1, 5, 7, 10, 11, 15, and 18 have been amended. Claims 1-8, 10-11, 15-16 and 18-19 are now pending.

### II. REJECTIONS UNDER 35 USC § 102

Claims 1-8, 10-12, and 14-19 stand rejected under 35 USC § 102(e) as being anticipated by U.S. Patent App. Pub. No. 2003/0028733 ("Tsunoda") with the Microsoft Press Computer Dictionary (MPCD) offered as extrinsic evidence. Applicant respectfully traverses these rejections insofar as they may apply to the currently pending claims because the cited art fails to teach or suggest every limitation of the claims.

For example, independent claim 1 as amended recites "a table memory configured to identify addresses within the nonvolatile memory array that have been recently accessed." With respect to the previous form of this limitation, the examiner cites Tsunoda ¶105, ¶107, and ¶130. Paragraphs 105 and 107 describe the use of a mapping table 603 to allocate portions of the volatile memory address space to logical sectors in a nonvolatile memory. There is no teaching or suggestion in Tsunoda that the mapping table should identify recently accessed portions of nonvolatile memory, and indeed, the implication is that the addresses in the mapping table are relatively static. Paragraph 130 describes the content of an "area management table 1601 [that] is prepared in the address mapping table" (¶127). The area management table includes an entry for tracking the number of times data in volatile memory has been updated after being copied from nonvolatile memory. However the number of updates does not correlate to time of access, and accordingly, neither the area management table nor the mapping table of Tsunoda is analogous to a table that identifies memory addresses that have been recently accessed. For at least this reason, independent claim 1 and its dependent claims 2-6 are allowable over the cited art.

Dependent claim 5 is amended to clarify that the read buffers can hold only a subset of the data in the memory region being buffered. With respect to

the previous version of this claim, the examiner cites Tsunoda ¶107, which describes the transfer of data from nonvolatile memory to a larger volatile memory. For at least this additional reason, claim 5 is allowable over the cited art.

Independent claim 7 as amended recites that "interface control module is further configured to update the table memory in response to the read commands." As previously mentioned, the implication in Tsunoda is that the mapping table is relatively static. No teaching or suggestion can be found of read buffers and a table memory having content that changes in response to read commands. For at least this reason, independent claim 7 and its dependent claim 8 are allowable over the cited art.

Independent claim 10 as amended recites limitations from canceled claim 12. Specifically, claim 10 recites "receiving a read command that comprises a read address; [and] determining whether data from the read address is buffered in a volatile read buffer." The examiner cites Tsunoda ¶50-52 as teaching these limitations. However, Tsunoda there describes functions for host control of the mapping and transfer of data from the nonvolatile memory to the volatile memory. Tsunoda does not here or elsewhere teach determining whether data from a received read address is stored in a volatile read buffer. For at least this reason, independent claim 10 and its dependent claim 11 are allowable over the cited art.

Independent claim 15 as amended recites "the buffered memory interface responsively stores, in a nonvolatile memory, one or more addresses of memory locations that have been recently accessed." With respect to a previous version of this limitation, the examiner cited Tsunoda ¶46-47 and 130, which describe tracking the number of times data in volatile memory has been updated after being copied from nonvolatile memory. However the number of updates is unrelated to the recentness with which a memory location has been accessed. For at least this reason, independent claim 15 and its dependent claims 16 and 18-19 are allowable over the cited art.

## III. EXAMINER INTERVIEW SUMMARY

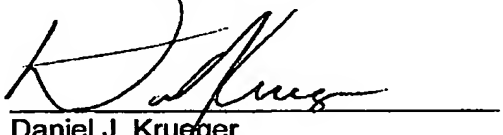
Applicant acknowledges with appreciation the examiner interview of August 23, 2006, in which the amendments to the independent claims were discussed with the undersigned attorney and the distinctions relative to Tsunoda were explained.

## IV. CONCLUSION

In the course of the foregoing discussions, applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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